IN THE SPECIFICATION:

1. Please amend the following paragraph starting at line 10, page 2 as follows:

In order to attain the object, shared memory data transfer apparatus according to a first aspect of the invention is shared memory data transfer apparatus where a plurality of masters (master 1, 5, 9, 13) access one shared memory (shared memory 20) to perform data transfers, the shared memory data transfer apparatus comprising a plurality of master interfaces (master I/Fs 2, 6, 10, 14) respectively connected to the master interfaces, write buffers ~~butters~~ (write data buffers 3, 7, 11, 15) connected to the master interfaces for retaining data written from the masters to the shared memory, read buffers ~~butters~~ (read data buffers 4, 8, 12, 16) connected to the master interfaces for retaining data read from the shared memory to the masters, a FIFO (command FIFO 18) provided between the master interfaces and the shared memory for storing commands from the masters directed to the shared memory in a first-in, first-out fashion, and a shared memory interface (shared memory I/F 19) for controlling data transfers from the write buffers to the shared memory or data transfers from the shared memory to the read buffers in accordance with commands fetched from the FIFO.